# PATENT ABSTRACTS OF JAPAN

(11)Publication number:

11-235029

(43) Date of publication of application: 27.08.1999

(51)Int.CI.

HO2M

HO2M 3/335 H02M 7/21

(21)Application number : 10-035740

(71)Applicant: TDK CORP

(22)Date of filing:

18.02.1998

(72)Inventor: AONUMA KENICHI

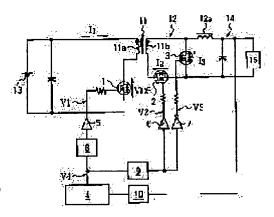
TAKAGI MASAKAZU

## (54) SWITCHING POWER SUPPLY

# (57)Abstract:

PROBLEM TO BE SOLVED: To control generation of loss and noise due to difference of the operation delay time of a switching element by providing a signal timing adjusting means so that the timing of input of the control signal to the first switching means is delayed from input of the control signal to the second and third switching means.

SOLUTION: A delay circuit 8 is arranged to the circuit between the control circuit 4 and drive circuit 5 of first switching element 1. An insulation circuit 9 connected to the drive circuits 6, 7 of the second and third switching elements 2, 3 is connected to the control circuit 4 between the control circuit 4 and delay circuit 8. The control signal V4 from the control circuit 4 is input in



direct to the drive circuits 6, 78 but input to the drive circuit 5 via a delay circuit 8. When a current I3 becomes zero, the third switching element 3 turns Off to impede a terminating current of the secondary coil 11b of transformer 11. Until the time when the current I2 starts to flow, the second switching element 2 is in the ON state. Therefore, the current 12 does flow into a parasitic diode and flows only through the channel between the drain and source of the element 2.

### **LEGAL STATUS**

[Date of request for examination]

16.11.1999

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or

application converted registration]

[Date of final disposal for application]

[Patent number]

3280615

[Date of registration]

22.02.2002

[Number of appeal against examiner's

decision of rejection]

[Date of requesting appeal against examiner's

decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office

(19)日本国特許庁 (JP)

# (12) 公開特許公報(A)

(11)特許山東公開發号

# 特開平11-235029

(43)公開日 平成11年(1999)8月27日

(51) Int.CL <sup>6</sup>		織別紀号	ΡI		
H02M	3/28		H02M	3/28	F
	3/335			3/335	В
	7/21			7/21	Α

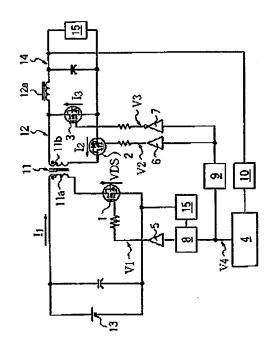
### 審査請求 未請求 請求項の数4 OL (全 7 頁)

(21)出顯番号	<b>特顯平10-35740</b>	(71)出顧人	000003067 ティーディーケイ株式会社
(22)出題日	平成10年(1998) 2 月18日		東京都中央区日本橋1丁目13番1号
		(72) 発明者	<b>青</b> 稻 賢一
			東京都中央区日本橋1丁目13番1号 ティース・ニュータングラング
		(Carly) Districted with	ーディーケイ株式会社内
		(化)%明督	高木 雅和 東京都中央区日本橋1丁目13番1号 ティ ーディーケイ株式会社内
		(74)代理人	弁理士 中村 稔 (外6名)

### (54)【発明の名称】 スイッテング電源装配

### (57)【要約】

【課題】 同期整流型スイッチング電鍵装置において、スイッチ回路のスイッチング素子と整流回路のスイッチング素子と整流回路のスイッチング素子の作助遅れ時間の钼速による損失及びノイズの発生を抑制できるスイッチング電源装置を提供すること。電源装置は、一次側のスイッチ手段と整流回路のスイッチ手段の間の耐圧特性の差に基づく作動遅れ時間の差を補償するため、該整流回路のスイッチ手段に副御信号が入力されるタイミングが遅くなるようにする信号タイミング調整手段を有する。この信号タイミング調整手段は、一次側スイッチ手段に入力される副御信号のタイミングを遅らす遅延手段として構成する。



. . ...

特闘平11-235029

(2)

#### 【特許請求の範囲】

【請求項1】 入力電圧を高周波電圧に変換する第1の スイッチ手段を有するスイッチ回路と、

前記スイッチ回路に1次巻線が接続され、2次巻線が出力回路に接続されたた変圧器と、を備え、前記出力回路は、前記変圧器の前記2次巻線に直列に接続された第2のスイッチ手段及び磁気素子と、前記2次巻線に並列に接続された第3スイッチ手段とからなる整流手段を有

出力電圧が所定の値となるように前記第1のスイッチ季 10 段をオン・オフ制御するため前記第1のスイッチ手段に与えられる制御信号を形成する制御手段が設けられ、前記第2のスイッチ手段は前記第1のスイッチ手段に与えられる制御信号と同期した前記制御手段からの信号でオン・オフ制御され、

前記第3のスイッチ手段は前記第1のスイッチ手段に与えられる制御信号とは逆のタイミングを有する前記制御手段からの信号でオン・オフ制御されるようになった、同期整施型電源装置であって、

前記第1のスイッチ手段と前記第2及び前記第3のスイッチ手段の間の耐圧特性又は電流容量の差に基づく作動遅れ時間の差を補値するため前記第2及び第3のスイッチ手段に制御信号が入力されるタイミングよりも前記第1のスイッチ手段に制御信号が入力されるタイミングが遅くなるようにする信号タイミング調整手段が設けられた。ことを特徴とする同期整流型スイッチング電鍵装

【語求項2】 語求項1に記載したスイッチング電源装置であって、前記信号タイミング調整手段は、前記第1 のスイッチ手段に入力される制御信号のタイミングを遅 30 らす返延手段であることを特徴とするスイッチング電源 装置、

【語求項3】 語求項2に記載したスイッチング電源装置であって、前記遅延手段は、前記第1スイッチ手段へのオン信号に対する遅延時間とオフ信号に対する遅延時間とを別々に設定できるようになったことを特徴とするスイッチング電源装置。

【語求項4】 請求項3に記載したスイッチング電源装置であって、負荷電流検出手段が設けられ、前記第1スイッチ手段へのオン信号に対する遅延時間が負荷電流の 40大きさに応じて変化させられるようになったことを特徴とするスイッチング電源装置。

【発明の詳細な説明】

[0001]

【産業上の利用分野】 本発明は、入力電圧をスイッチ 手段によりスイッチングして高周波電圧に変換し、この 高周波電圧を変圧器により変圧し、整流して任意の出力 電圧を出力するスイッチング電源装置に関する。特に本 発明は、出力部の整流回路の整流素子としてスイッチ手 限を設け、並スイッチ手段を入力回路のスイッチ手段の 作動と同期して作動させるようにした同期整流型スイッチング電源装置に関する。

[0002]

【従来技術】 入力電圧をスイッチ手段により高層波電 圧に変換して変圧器の1次巻線に印刷し、この変圧器の 2次巻線を整流回路を有する出力回路から直流出力とし て取り出すようにしたスイッチング電源装置はよく知ら れている。このスイッチング電源装置においては、整流 回路は、変圧器の2次巻線に直列に接続されたダイオー 下等の整流素子とコイル等の磁気素子、及び、2次巻線 に並列に接続され別の整流素子を備える。入力側のスイ ッチ手段は、出力電圧が所定の値となるように副御回路 からの制御信号によりオン・オフ制御される。この形式 のスイッチング電源装置において、ダイオードに固有の 順方向降下電圧による損失を軽減するためにダイオード に代えてスイッチ素子を使用し、これらのスイッチ素子 を入力側のスイッチ手段と同期させてオン・オフ副御す るようにした構成が、同期整流型スイッチ電源装置とし て知られており、これらの形式のスイッチ電源装置の代 表的なものは、特闘平4-4750号公報、特闘平5-260738号 公報及び特関平7-194104号公報、並びに米国特許第4,87 9,555 号明細茎に記載されている。

【①003】図5に、従来の同期整流型スイッチ電源装 置の一例を示す。図5において、電源13は変圧器11 の一次巻線11aに接続され、該一次巻線11aにはさ らにFET型のスイッチ素子lが接続される。変圧器l 1の二次側巻線11りには、整流回路12を有する出力 回路14が接続され、該出力回路14は負債15に接続 される。整流回路12は、変圧器11の二次巻線11b に直列に接続された第2のスイッチ素子2と磁気素子す なわちインダクタ12aを備える。また、整流回路12 は、変圧器!1の二次巻線11bに並列に接続された第 3のスイッチ素子3を備える。スイッチ素子1.2、3 を副御するために制御回路4が設けられている。副御回 路4は、フォトカプラ又は変圧器などで構成される絶縁 回路9或いは負荷弯圧検出回路10を介して出力回路1 4に接続されており、出力電圧が一定になるようにパル ス帽を変調した。スイッチ素子!を副御するための制御 信号V4を出力する。制御回路4の出力V4は、駆動回 | 路5を介して出力V1として第1のスイッチ素子1のゲ ート電極に印加される。副御回路4からの制御信号V4 は又、変圧器又はフォトカプラなどで構成された絶縁回 路9を介して駆動回路6、7に接続される。駆動回路6 は、第1のスイッチ素子1に印加される出力V1と同じ 極性の出力V2を第2のスイッチ素子2のゲート電極に 印加する。駆動回路7は 第1のスイッチ素子1に印加 される出力V1とは逆極性の出力V3を第3のスイッチ 素子3のゲート電極に印加する。

発明は、出力部の整液回路の整液素子としてスイッチ手 【①①①4】周知のように、制御回路4からの副御信号 段を設け、該スイッチ手段を入力回路のスイッチ手段の 50 により第1のスイッチ素子1がオン・オフ制御されて電 源13からの電圧を高周波電圧とし、この高周波電圧が 変圧器11の一次巻線に印刷される。変圧器11の二次 巻線11りに発生する電圧は整流回路12により整流さ れて出力回路 14から出力される。出力回路 14の出力 湾圧は負荷湾圧検出回路 1 ()により検出されて制御回路 4に入力される。制御回路4は、出力電圧が所定の値と なるように第1のスイッチ素子1を制御するための制御 信号を生成する。整施回路12において、第1のスイッ チ素子1がオン状態のときは第2のスイッチ素子2もオ ン状態となり、第3のスイッチ素子3はオフ状態にな る。第1のスイッチ素子1がオフになると、第の2スイ ッチ素子2もオフになり、第3スイッチ素子3はオンに なる.

3

【0005】ここで、第1. 第2、第3のスイッチ素子 1.2、3に同じタイミングで制御信号が印加される場 合には、スイッチ素子を構成するFETの作動特性のた めに、各スイッチ素子間で動作のタイミングにずれを生 じる。すなわち、スイッチ素子のゲート電極に駆動電圧 が印加されてから該スイッチ素子を流れるドレイン電流 が定常値に達するまでの動作遅れ時間及びゲート電極に 印加される電圧が絶たれてからドレイン電流が流れなく なるまでの動作遅れ時間がある。この遅れ時間のため に、スイッチング電源装置の効率が低下する。この点を 詳細に説明すると、入力側は電圧が高いために、入力側 のスイッチ素子 1 を構成するFETは、一般に耐圧が比 較的高く、電流容置の小さいものが使用される。したが って、このスイッチ素子1は、ゲート電極に駆動電圧が 印刻されてからオン状態となるまでの遅れ時間及び駆動 電圧が除去されてからオフ状態となるまでの遅れ時間が 比較的短い。これに対して、出力側は電圧が低く、出力 30 側のスイッチ素子2、3を構成するFETは、一般に耐 圧が低く電流容量の大きいものが使用される。このた め、これちスイッチ素子2、3においては、ゲート電極 に駆動電圧が印刻されてからオン状態となるまでの遅れ 時間及び駆動電圧が除去されてからオフ状態となるまで の遅れ時間が比較的長い。

【0006】図5に示すスイッチング電源装置の各部の 電圧又は電流波形を図6に示す。時刻t。で制御信号V 4がローからハイになると、駆動回路5からの出力V1 と駆動回路6からの出力V2が同時にハイになる。ま た、駆動回路?からの出力V3は同じタイミングでロー になる。この時刻し、からスイッチング素子の作動特性 に応じた遅れ時間の後、時刻 t 、 でスイッチング素子 1 がオンになり、電流!、が変圧器11の一次側巻線11 aに流れる。同時に、変圧器11の二次側巻線11bに 電流 I 、が発生する。スイッチング素子1のオフ状態で スイッチング素子3に流れていた電流 1。は、時刻 t。 で減少し始め、時刻も、でゼロになる。素子の特性上、 スイッチング素子3の作動遅れ時間はスイッチング素子 1の遅れ時間より長いので、この時点ではスイッチング 50 値するため第2及び第3のスイッチ手段に制御信号が入

素子3はまだオン状態にある。したがって、変圧器11 の二次巻線11bは、スイッチング素子2、3を介して 短絡状態となり、大きな短絡電流が流れ、効率低下及び ノイズの原因となる。また、スイッチング素子2も作動 遅れ時間がスイッチング素子!よりも長いので、この時 点では、スイッチング素子2はオフ状態にある。そのた め、該スイッチング素子2を通って流れる短絡電流は、 ドレイン・ソース間のチャンネルではなく、内部の寄生 ダイオードを通ることになるので、損失が大きくなる。 10 図6において、電流! のうち寄生ダイオードに流れる 電流を斜線で示す。

【0007】時刻も、で副御信号V4がハイからローに なると、駆動回路5からの出力V!と駆動回路6からの 出力V2がローになる。 駆動回路の出力V3は同じタイ ミングでローからハイになる。時刻も、からスイッチン グ素子の作動特性に応じた遅れ時間の後、時刻も。でス イッチング素子1がオフになり、電流1、、1。が減少 し始め、電流上、が増加し始める。このとき、スイッチ ング素子3はまだオン状態でないため、該スイッチング 素子3には寄生ダイオードを通って電流が流れるように なり、損失が大きくなる。図6に、電流!。のうち、寄 生ダイオードに流れる電流を視線で示す。

#### 180001

【発明が解決しようとする課題】 本発明は、上述した 形式の同期整流型スイッチング電鍵装置において、スイ ッチ回路のスイッチング素子と整液回路のスイッチング 素子の作動遅れ時間の相違による損失及びノイズの発生 を抑制できるスイッチング電源装置を提供することを解 決すべき課題とする。

#### [0009]

【課題を解決するための手段】 上記課題を解決するた めの本発明によるスイッチング電源装置は、入力電圧を 高周波電圧に変換する第1のスイッチ手段を有するスイ ッチ回路と、該スイッチ回路に1次巻線が接続され、2 次巻線が出力回路に接続されたた変圧器と、を備え、該 出方回路は、変圧器の2次巻線に直列に接続された第2 のスイッチ手段及び磁気素子と、2次巻線に並列に接続 された第3スイッチ手段とからなる整流手段を有し、出 力電圧が所定の値となるように第1のスイッチ手段をオ ン・オフ制御するため該第1のスイッチ手段に与えられ る副御信号を形成する制御手段が設けられ、第2のスイ ッチ手段は第1のスイッチ手段に与えられる制御信号と 同期した制御手段からの信号でオン・オフ制御され、第 3のスイッチ手段は第1のスイッチ手段に与えられる制 御信号とは逆のタイミングを有する調御手段からの信号 でオン・オフ副御されるようになった。同期整流型の装 置である。本発明の電源装置は、その特徴として、第1 のスイッチ手段と第2及び第3のスイッチ手段の間の耐 圧特性又は電流容置の差に基づく作動遅れ時間の差を結 力されるタイミングよりも第1のスイッチ手段に副御信号が入力されるタイミングが遅くなるようにする信号タイミング調整手段を有する。この信号タイミング調整手段は、第1のスイッチ手段に入力される制御信号のタイミングを遅らす返延手段として構成することが最も望ましい。この場合。該遅延手段は、第1スイッチ手段へのオン信号に対する遅延時間とオフ信号に対する遅延時間とを別々に設定できるようにすることが好ましい。本発明のさらに好ましい感傷においては、負荷電流後出手段を設け、第1スイッチ手段へのオン信号に対する遅延時間が負荷電流の大きさに応じて変化させられるようにす

5

【0010】本発明のスイッチング電源装置においては、上述のように、信号タイミング調整手段により、第1のスイッチ手段と第2及び第3のスイッチ手段の間の耐圧特性の差に基づく作動返れ時間の差を結償するため第2及び第3のスイッチ手段に制御信号が入力されるタイミングよりも第1のスイッチ手段に副御信号が入力されるタイミングが遅くなるように調整するので、第1、第2、第3スイッチング素子のオン・オフタイミングを20完全に同期させることができ、スイッチング素子の寄生ダイオードに流れる電流を減少させて損失を低下させ、ノイズの発生を抑制することができる。

#### [0011]

【実施例】 以下、本発明の実施例を図について説明す る。先ず図1を参照すると、ここに示された実施例の回 「路は、図5に示す従来の回路と、構成及び作用ともほぼ 同一で、対応する部分は同一の符合を付して詳細な説明 を省略する。この実施例の回路では、副御回路4から第 1のスイッチング素子1の駆動回路5に至る回路に遅延 30 回路8が配置される。第2. 第3のスイッチング素子 2. 3の駆動回路6、7に接続される絶縁回路9は、制 御回路4と遅延回路8の間で制御回路4に接続される。 したがって、副御回路4からの制御信号V4は、駆動回 路6.7には直接入力されるが、駆動回路5には遅延回 路8を経て入力される。図2に、図1に示す回路の各部 の電圧又は電流波形を示す。時刻t,で制御信号V4が ローからハイになると、駆動回路6からの出力V2がハ イになり、同時に、駆動回路7からの出力V3は同じタ イミングでローになる。第1のスイッチング素子1の躯 40 動回路5には、副御信号V4が時間△T、だけ遅れて入 力されるので、駆動回路5の出力V、は、時刻も。より 時間△下、だけ遅れた時刻も、でローからハイになる。 スイッチング素子!は時刻も。から該スイッチング素子 の動作特性に応じた遅れ時間の後、時刻も、でオンにな り、電流!、が変圧器!1の一次巻線11aに流れ、同 時に、変圧器11の二次巻線11bに電流1,が発生す る。スイッチング素子1のオフ状態でスイッチング素子 3に流れていた電流!。は時刻 t , で減少し始め、時刻

値に達する。スイッチング素子3は時刻1。から該スイッチング素子の作動特性に応じた遅れ時間の後、時刻1。でオフする。△T、は時刻1。でスイッチ素子3がオフするように定められている。一般にスイッチング素子における作動遅れ時間は、オフする時の方がオンする時間が長いので、スイッチング素子2は時刻1。よりも早い時点でオンになっている。

【0012】この回路においては、時刻t』で電流!』 ゼロになるとき、第3のスイッチング素子3もオブにな るので、変圧器11の二次巻線11bに短絡電流が流れ るのを阻止できる。電流1、が流れ始める時刻も、まで に第2のスイッチング素子2はオン状態になっているの で、電流1、は素子2のドレイン・ソース間のチャンネ ルを流れ、寄生ダイオードには電流はほとんど流れな い。とのようにして、本発明のこの実施例では、損失を 低減し、ノイズを減少させることができる。時刻も、で 制御信号V4がハイからローになると、駆動回路6の出 カV2がローになる。駆動回路の出力V3も同じタイミ ングでローからハイになる。第1のスイッチング素子1 の駆動回路5の出力V1は、時刻t、から時間△T。だ け遅れた時刻も、でハイからローになる。この時刻も、 からスイッチング素子の作動特性に応じた遅れ時間の 後、時刻し。でスイッチング案子1がオフになり、電流 1, 1, が減少し始め、電流1, が増加し始める。時 聞△T」は、第1のスイッチング素子1がオン状態から オフ状態になる場合の作動遅れ時間と第3のスイッチン グ索子3がオフ状態からオン状態になる場合の作動遅れ 時間の差に対応するように定めてあるので、時刻も。で スイッチング素子1がオフになるときには、スイッチン グ素子3はすでにオン状態になっており、該スイッチン グ索子3には寄生ダイオードを通って電流はほとんど流 れない。

【0013】一般に、スイッチング素子における作動遅れ時間は、オフする時の方がオンする時より長い。したがって、この実施例では、第2のスイッチング素子2がオフするタイミングは、時刻し。より遅れた時刻し、となる。したがって、電流 Li は時刻し、までスイッチング素子2のチャンネルを流れることができ、寄生ダイオードに流れることはない。上述の実施例において、制御信号 V 4 がローからハイになる場合の遅延回路の遅れ時間 ム T、と、副御信号 V 4 がハイからローになる場合の遅延回路の遅れ時間 ム T、は、それぞれ別個に適定することが望ましいが、同じ値にしても相当程度の効果を達成することができる。なお、回路の構成、入力状態或いはスイッチング素子の特性によっては、制御信号 V 4 がハイからローになる場合の遅延回路の遅れ時間 ム T、はゼロとしてもよい。

る。スイッチング素子1のオフ状態でスイッチング素子 [0014] 図3に本発明の他の実施例を示す。この実 3に流れていた電流1。は時刻t , で減少し始め、時刻 施例では、制御回路4は変圧器11の二次側回路内に配 t , でゼロになる。時刻t , では電流 I , 、 I , も定常 50 置されており、該制御回路4からの制御信号V4は、絶 (5)

縁回路を経ずに直接に駆動回路6、7に入力される。そ の他の点では、この実施例は図1の実施例と同様であ り 作動も同じである。図4は、本発明のさらに別の実 施例を示す。この実施例では、変圧器11の一次側回路 に電流検出回路15が設けられる。この電流検出回路1 5は遅延回路8に接続され、出力電流の減少に応じて遅 れ時間△T、が大きくなり、出力電流の増加に応じて遅 れ時間ム丁、が小さくなるように遅延回路8を副御す る。図1の実施例の構成では、負荷電流が減少すると、 電流 [ が定常値からゼロになる時刻及び電流 [ 、 ! ,がゼロから定常値になる時刻は、も,より早くなり、 時刻t, に近づく。ところが、第3のスイッチング素子 3がオフする時刻は、1,のままであるので、スイッチ ング素子3がオン状態を継続している間にスイッチング 素子1、2がオン状態になる。このため、変圧器11の 二次側巻線を通る回路には、スイッチング素子2、3を 介して短絡電流が流れ、ノイズ発生の原因となる。図4 の実施例は、出力電流に応じて遅れ時間を制御するの で、この問題を解消することができる。

7

【① 0 1 5 】本発明の構成により達成できる効率改善を 20 置を示す回路図である。 特定の例について試算した。仮定として、従来の回路に おいては、スイッチング素子の動作遅れの違いにより、 スイッチング素子の寄生ダイオードに211 nSの間電流が 流れ、寄生ダイオードにおける電圧降下は0.9 Vとす る。電源装置の仕様は、V。=3.3 V. (。=15A、駆 動周波数を250 k目でとし、スイッチング素子の導通状 麼での抵抗値を5.7mΩとする。ダイオードで整流回路を 模成した場合の効率を75%とすると、このダイオードを FET 型のスイッチング素子に置き換えた整流回路を備え る同期整流型スイッチング電源装置の効率は、82.9%と 30 る。 なり、図1に示す本発明の実施例の装置の効率は83.9% になる。この計算においては、本発明により得られる効 果のうち、スイッチング素子の作動遅れを縞礁すること により得られる効率の改善のみを考慮したものである。 本発明においては、この他に、短絡電流に起因する損失 の改善効果が達成され、ノイズ軽減効果も顕著である。 【りり16】図?に、上述の計算に用いた仕様の回路に おける作動遅れ時間△丁。をゼロとし、△丁。を変化さ せた場合の効率の変化と、短絡電流及びリカバリ電流の 変化を示す。ここで、短絡電流及びリカバリ電流は、第 40

3のスイッチング素子3を流れる電流 1, のうち、矢印 と反対方向に流れる電流を指す。この図から、遅延時間 を増加させると、短絡電流が減少し、効率が約5%改善 されることが分かる。この効率改善には、第2のスイッ チング素子2の作動遅れの補償が寄与する部分もある。 遅延時間が大きくなり過ぎると、電流 1. が流れている ときに第3のスイッチング素子3がオフする状態を生じ るので、電流1,が寄生ダイオードを流れることにな り、効率が低下する。寄生ダイオードに電流!。が流れ - ている途中で第1のスイッチング素子1がオンになる と、第3のスイッチング素子3の寄生ダイオードにリカ バリ電流が流れる。このリカバリ電流は遅延時間に比例 して増加し、効率を悪くする原因になる。

【()() 17】なお、図4の実施例において、負荷電流の 検出に、変圧器11の一次側回路に接続した電流検出回 路15を用いたが、この電流検出回路15は、変圧器1 1の二次側回路に設けてもよい。

【図面の簡単な説明】

【図1】 本発明の一実施例によるスイッチング電源装

【図2】 図1の回路における各部の電圧又は電流の波 形を示す波形図である。

【図3】 本発明の他の実施例によるスイッチング電源 装置を示す図1と同様な回路図である。

【図4】 本発明のさらに他の実施例によるスイッチン グ電源装置を示す図1と同様な回路図である。

【図5】 従来の同期整流型スイッチング電源装置の一 例を示す図1と同様な回路図である。

【図6】 図5の回路における各部の波形を示す図であ

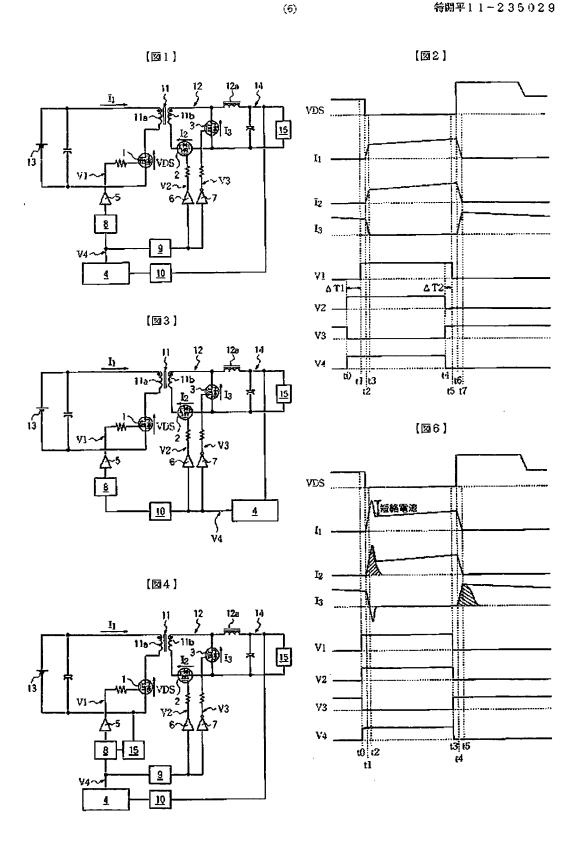
【図?】 本発明に実施例における遅延時間により得ら れる効率の改善と短絡電流及びリカバリ電流の変化を示 す図表である。

【符合の説明】

1.2、3・・・スイッチング素子.4・・・副御回 路. 5、6、7・・・駆動回路、8・・・遅延回路、9 ・・・絶縁回路、10・・・負荷電圧負出回路、11・ ・・変圧器、12・・・整流回路、13・・・電源、1 4・・・出力回路、15・・・負荷

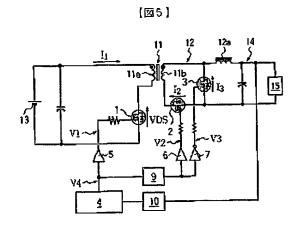
1/20/04

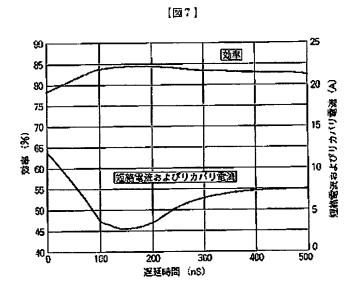
特関平11-235029



(7)

特開平11-235029 ·





特関平11-

【公報種別】特許法第17条の2の規定による補正の掲載 【部門区分】第7部門第4区分

【発行日】平成13年6月22日(2001.6.22)

【公開香号】特開平11-235029

【公開日】平成11年8月27日(1999.8.27)

【年通号数】公開特許公報11-2351

【出願香号】特願平10-35740

【国際特許分類第7版】

H02M 3/28 3/335

7/21

[FI]

HO2M 3/28

3/335 E

7/2**1** /

# 【手続緒正書】

【提出日】平成11年11月16日(1999. 11. 16)

【手続舖正1】

【補正対象書類名】明細書

【補正対象項目名】特許請求の疑問

【補正方法】変更

【補正内容】

【特許請求の箇囲】

【語求項 1 】 入力電圧を高周波電圧に変換する第 1 の スイッチ手段を有するスイッチ回路と

前記スイッチ回路に1次巻線が接続され、2次巻線が出 力回路に接続されたた変圧器と、

を備え、前記出方回路は、前記変圧器の前記2次巻線に 直列に接続された第2のスイッチ手段及び遊気素子と、 前記2次巻線に並列に接続された第3スイッチ手段とか ちなる整流手段を有し、

出力電圧が所定の値となるように前記第1のスイッチ手段をオン・オフ制御するため前記第1のスイッチ手段に 与えられる制御信号を形成する制御手段が設けられ、

前記第2のスイッチ手段は前記第1のスイッチ手段に与えられる制御信号と同期した前記制御手段からの信号でオン・オフ制御され。

同期整義型電源装置であって、

前記第1のスイッチ手段と前記第2及び ッチ手段の間の耐圧特性又は電流容量の; 遅れ時間の差を補償するため前記第2及; チ手段に制御信号が入力されるタイミン 1のスイッチ手段に制御信号が入力され。 遅くなるようにする信号タイミング調整: た、ことを特徴とする同期整流型スイッ 置。

【請求項2】 請求項1に記載したスイ 置であって、前記信号タイミング調整手 のスイッチ手段に入力される制御信号の ちず遅延手段であることを特徴とするス 装置。

【請求項3】 請求項2に記載したスイ 置であって、前記遅延手段は、前記第1. のオン信号に対する遅延時間とオフ信号 間とを別々に設定できるようになったと スイッチング電源装置。

【請求項4】 請求項3に記載したスイ 置であって、負荷電液検出手段が設けら イッチ手段へのオン信号に対する遅延時

## Japanese Patent Application Publication No. 11-235029

### \* NOTICES \*

Japan Patent Office is not responsible for any

damages caused by the use of this translation.

- 1. This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

### **CLAIMS**

### [Claim(s)]

over an off signal.

[Claim 1] A switching circuit which has the 1st switching means which changes input voltage into high-frequency voltage, It has \*\*\*\*\*\* by which a primary coil was connected to said switching circuit, and a secondary coil was connected to an output circuit. Said output circuit The 2nd switching means and magnetic cell which were connected to said secondary coil of said transformer at a serial, It has a rectification means which becomes said secondary coil from the 3rd switching means connected to juxtaposition. A control means which forms a control signal given to said 1st switching means in order to carry out on-off control of said 1st switching means so that output voltage may serve as a predetermined value is established. On-off control of said 2nd switching means is carried out by signal from said control means which synchronized with a control signal given to said 1st switching means. On-off control of said 3rd switching means came to be carried out to a control signal given to said 1st switching means by signal from said control means which has timing of reverse. It is a synchronous detection mold power unit. In order to compensate a difference of an actuation time delay based on said 1st switching means, said 2nd [the] and a resisting pressure property between said 3rd switching means, or a difference of current capacity Synchronous detection mold switching telegraph-key equipment characterized by what a signal timing adjustment means to make it timing as which a control signal is inputted into said 1st switching means rather than timing as which a control signal is inputted into said 2nd and 3rd switching means become late was established for. [Claim 2] It is switching power supply equipment characterized by being a delay means to delay the timing of a control signal of being switching power supply equipment indicated to claim 1, and inputting said signal timing adjustment means into said 1st switching means. [Claim 3] It is switching power supply equipment characterized by the ability to set up now independently a time delay [ as opposed to / are switching power supply equipment indicated to claim 2, and / an ON signal to said 1st switching means in said delay means ], and a time delay

[Claim 4] Switching power supply equipment characterized by being switching power supply equipment indicated to claim 3, establishing a load current detection means, and coming to

JP 11-235029 Pg 1 of 20

change a time delay over an ON signal to said 1st switching means according to magnitude of the load current.

JP 11-235029 Pg 2 of 20

### **DETAILED DESCRIPTION**

[Detailed Description of the Invention] [0001]

[Industrial Application] This invention switches input voltage by the switching means, changes it into high-frequency voltage, and relates to the switching power supply equipment which transforms this high-frequency voltage with a transformer, rectifies and outputs the output voltage of arbitration. Especially this invention establishes a switching means as a rectifying device of the rectifier circuit of the output section, and relates to the synchronous detection mold switching power supply equipment it was made to operate this switching means synchronizing with actuation of the switching means of an input circuit.

[0002]

[Description of the Prior Art] Input voltage is changed into high-frequency voltage by the switching means, it is impressed by the primary coil of a transformer, and the switching power supply equipment which took out the secondary coil of this transformer from the output circuit which has a rectifier circuit as a dc output is known well. In this switching power supply equipment, it connects with a rectifying device, magnetic cells, such as a coil, and secondary coils, such as diode connected to the secondary coil of a transformer at the serial, at juxtaposition, and a rectifier circuit is equipped with another rectifying device. On-off control of the switching means of an input side is carried out by the control signal from a control circuit so that output voltage may serve as a predetermined value. In the switching power supply equipment of this format, in order to mitigate loss by the forward drop voltage of a proper to diode, it replaces with diode and a switching device is used, the configuration which these switching devices are synchronized with the switching means of an input side, and was made to carry out on-off control is known as a synchronous detection mold switch power unit, and the typical thing of the switch power unit of such format is indicated by JP,4-4750,A, JP,5-260738,A and JP,7-194104,A, and the list at the U.S. Pat. No. 4,870,555 description.

[0003] An example of the conventional synchronous detection mold switch power unit is shown in drawing 5. In drawing 5, a power supply 13 is connected to primary-winding 11a of a transformer 11, and the switching device 1 of an FET mold is further connected to this primarywinding 11a. The output circuit 14 which has a rectifier circuit 12 is connected to secondary coil 11b of a transformer 11, and this output circuit 14 is connected to a load 15. A rectifier circuit 12 is equipped with 2nd switching device 2 and magnetic cell, i.e., inductor, 12a connected to secondary-winding 11b of a transformer 11 at the serial. Moreover, a rectifier circuit 12 is equipped with the 3rd switching device 3 connected to juxtaposition at secondary-winding 11b of a transformer 11. In order to control switching devices 1, 2, and 3, the control circuit 4 is formed. It connects with the output circuit 14 through the insulating circuit 9 or the load voltage detector 10 which consists of a photo coupler or a transformer, and a control circuit 4 outputs the control signal V4 for controlling a switching device 1 which modulated pulse width so that output voltage might become fixed. The output V4 of a control circuit 4 is impressed to the gate electrode of the 1st switching device 1 as an output V1 through the actuation circuit 5. The control signal V4 from a control circuit 4 is connected to the actuation circuits 6 and 7 again through the insulating circuit 9 which consisted of a transformer or a photo coupler. The actuation circuit 6 impresses the same polar output V2 as the output V1 impressed to the 1st switching device 1 to the gate electrode of the 2nd switching device 2. The actuation circuit 7

JP 11-235029 Pg 3 of 20

impresses the output V3 of reversed polarity to the gate electrode of the 3rd switching device 3 with the output V1 impressed to the 1st switching device 1.

[0004] As everyone knows, on-off control of the 1st switching device 1 is carried out by the control signal from a control circuit 4, voltage from a power supply 13 is made into highfrequency voltage, and this high-frequency voltage is impressed to the primary winding of a transformer 11. It is rectified by the rectifier circuit 12 and the voltage generated in secondarywinding 11b of a transformer 11 is outputted from an output circuit 14. The output voltage of an output circuit 14 is detected by the load voltage detector 10, and is inputted into a control circuit 4. A control circuit 4 generates the control signal for controlling the 1st switching device 1 so that output voltage serves as a predetermined value. In a rectifier circuit 12, when the 1st switching device 1 is an ON state, the 2nd switching device 2 will also be in an ON state, and the 3rd switching device 3 is turned off. If the 1st switching device 1 becomes off, the 2 switching devices 2 of \*\* will also become off, and the 3rd switching device 3 will be turned on. [0005] Here, when a control signal is impressed to the same timing as the 1st, 2nd, and 3rd switching device 1, 2, and 3, a gap is produced to timing of operation between each switching device for the operational characteristic of FET which constitutes a switching device. That is, there is a time delay of operation after the voltage impressed to a time delay of operation and a gate electrode until the drain current which flows this switching device after driver voltage is impressed to the gate electrode of a switching device reaches a steady-state value is severed until drain current will not flow. The effectiveness of switching power supply equipment falls for this time delay. If this point is explained to details, since voltage of an input side is high, generally FET which constitutes the switching device 1 of an input side will have comparatively high pressure-proofing, and what has small current capacity will be used. Therefore, this switching device 1 has a comparatively short time delay after a time delay and driver voltage after driver voltage is impressed to a gate electrode until it will be in an ON state are removed until it will be in an OFF state. On the other hand, voltage of an output side is low and, generally, as for FET which constitutes the switching devices 2 and 3 of an output side, the thing with low pressureproofing which has large current capacity is used. For this reason, in these switching devices 2 and 3, a time delay after a time delay and driver voltage after driver voltage is impressed to a gate electrode until it will be in an ON state are removed until it will be in an OFF state is comparatively long.

[0006] The voltage or the current wave form of each part of switching power supply equipment shown in drawing 5 is shown in drawing 6. Time of day to If a control signal V4 becomes a high from a low, the output V1 from the actuation circuit 5 and the output V2 from the actuation circuit 6 will become a high simultaneously. Moreover, the output V3 from the actuation circuit 7 becomes a low to the same timing. this time of day t0 from -- after the time delay according to the operational characteristic of a switching element, and time of day t1 A switching element 1 is turned on and current I1 flows to upstream coil 11a of a transformer 11. Simultaneously, it is current I2 to secondary coil 11b of a transformer 11. It generates. Current I3 which was flowing to the switching element 3 by the OFF state of a switching element 1 Time of day t1 It begins to decrease and is time of day t2. It becomes zero. On the property of an element, since the actuation time delay of a switching element 3 is longer than the time delay of a switching element 1, at this event, a switching element 3 is still in an ON state. Therefore, secondary-winding 11b of a transformer 11 will be in a short circuit condition through switching elements 2 and 3, and a big short-circuit current flows and it causes degradation and a noise. Moreover, since the actuation time delay is longer than a switching element 1, at this event, a switching

JP 11-235029 Pg 4 of 20

element 2 also has a switching element 2 in an OFF state. Therefore, since the short-circuit current which flows through this switching element 2 will pass not along the channel between the drain sources but along internal parasitism diode, loss becomes large. It sets to <u>drawing 6</u> and is current I2. A slash shows the current which flows to parasitism diode inside.

[0007] Time of day t3 If a control signal V4 becomes a low from a high, the output V1 from the actuation circuit 5 and the output V2 from the actuation circuit 6 will become a low. The output V3 of an actuation circuit becomes a high from a low to the same timing. time of day t3 from -- after the time delay according to the operational characteristic of a switching element, and time of day t4 a switching element 1 -- off -- becoming -- current I1 and I2 decreasing -- beginning -- current I3 It begins to increase. Since a switching element 3 still is not an ON state at this time, to this switching element 3, current comes to flow through parasitism diode, and loss becomes large. To drawing 6, it is current I3. A look shows the current which flows to parasitism diode inside.

[8000]

[Problem(s) to be Solved by the Invention] This invention makes it to offer the switching power supply equipment which can control the loss by difference of the actuation time delay of the switching element of a switching circuit and the switching element of a rectifier circuit, and generating of a noise the technical problem which should be solved in the synchronous detection mold switching telegraph-key equipment of the format mentioned above. [0009]

[Means for Solving the Problem] Switching power supply equipment by this invention for solving the above-mentioned technical problem A switching circuit which has the 1st switching means which changes input voltage into high-frequency voltage, It has \*\*\*\*\*\* by which a primary coil was connected to this switching circuit, and a secondary coil was connected to an output circuit. This output circuit The 2nd switching means and magnetic cell which were connected to a secondary coil of a transformer at a serial, It has a rectification means which becomes a secondary coil from the 3rd switching means connected to juxtaposition. A control means which forms a control signal given to this 1st switching means in order to carry out on-off control of the 1st switching means so that output voltage may serve as a predetermined value is established. On-off control of the 2nd switching means is carried out by signal from a control means which synchronized with a control signal given to the 1st switching means. A control signal with which the 3rd switching means is given to the 1st switching means is equipment of a synchronous detection mold by which on-off control came to be carried out by signal from a control means which has timing of reverse. A power unit of this invention has a signal timing adjustment means to make it timing as which a control signal is inputted into the 1st switching means rather than timing as which a control signal is inputted into the 2nd and 3rd switching means become late in order to compensate a difference of an actuation time delay based on a resisting pressure property between the 1st switching means and the 2nd and 3rd switching means, or a difference of current capacity as the feature. As for this signal timing adjustment means, it is most desirable to constitute as a delay means to delay timing of a control signal inputted into the 1st switching means. In this case, as for this delay means, it is desirable to enable it to set up independently a time delay over an ON signal to the 1st switching means and a time delay over an off signal. A load current detection means is established and it is made for a time delay over an ON signal to the 1st switching means to be changed in a still more desirable mode of this invention according to magnitude of the load current.

[0010] In switching power supply equipment of this invention as mentioned above with a signal

JP 11-235029 Pg 5 of 20

timing adjustment means In order to compensate a difference of an actuation time delay based on a difference of a resisting pressure property between the 1st switching means and the 2nd and 3rd switching means Since it adjusts so that timing as which a control signal is inputted into the 1st switching means rather than timing as which a control signal is inputted into the 2nd and 3rd switching means may become late On--off timing of the 1st, 2nd, and 3rd switching element can be synchronized thoroughly, current which flows to parasitism diode of a switching element can be decreased, loss can be reduced, and generating of a noise can be controlled. [0011]

[Example] Hereafter, the example of this invention is explained about drawing. If <u>drawing 1</u> is referred to first, the circuit of the example shown here is almost the same as that also of the conventional circuit shown in drawing 5, and a configuration and an operation, and a corresponding portion will attach the same agreement and will omit detailed explanation. In the circuit of this example, a delay circuit 8 is arranged in the circuit from the control circuit 4 to the actuation circuit 5 of the 1st switching element 1. The insulating circuit 9 connected to the actuation circuits 6 and 7 of the 2nd and 3rd switching element 2 and 3 is connected to a control circuit 4 between a control circuit 4 and a delay circuit 8. Therefore, although the direct input of the control signal V4 from a control circuit 4 is carried out to the actuation circuits 6 and 7, it is inputted into the actuation circuit 5 through a delay circuit 8. The voltage or the current wave form of each part of a circuit shown in drawing 2 at drawing 1 is shown. Time of day to If a control signal V4 becomes a high from a low, the output V2 from the actuation circuit 6 will become a high, and the output V3 from the actuation circuit 7 will become a low to the same timing simultaneously, the actuation circuit 5 of the 1st switching element 1 -- a control signal V4 -- time amount deltaT1 only -- since it is behind and is inputted -- output V1 of the actuation circuit 5 Time of day to Time amount deltaT1 only -- overdue time of day t1 from a low -- yes, it comes to be alike a switching element 1 -- time of day t0 from -- after the time delay according to the operating characteristic of this switching element, and time of day t2 ON -- becoming -current I1 Primary-winding 11a of a transformer 11 flowing -- simultaneous -- secondarywinding 11b of a transformer 11 Current I2 It generates. Current I3 which was flowing to the switching element 3 by the OFF state of a switching element 1 Time of day t2 It begins to decrease and is time of day t3. It becomes zero. Time of day t3 It is current I1 and I2 then. A steady-state value is reached. a switching element 3 -- time of day to from -- after the time delay according to the operational characteristic of this switching element, and time of day t3 It turns off. \*\*T1 Time of day t3 It is determined that a switching device 3 turns off. Since the time amount which the direction when turning off the actuation time delay in a switching element turns on is generally long, a switching element 2 is time of day t2. It is turned on when early. [0012] It sets in this circuit and is time of day t3. Current I3 Since the 3rd switching element 3 also becomes off when becoming zero, it can prevent that a short-circuit current flows to secondary-winding 11b of a transformer 11. current I2 Time of day t2 which begins to flow by -since the 2nd switching element 2 is turned on -- current I2 Flowing the channel between the drain sources of an element 2, to parasitism diode, current hardly flows. Thus, in this example of this invention, loss can be reduced and a noise can be decreased. Time of day t4 If a control signal V4 becomes a low from a high, the output V2 of the actuation circuit 6 will become a low. The output V3 of an actuation circuit also becomes a high from a low to the same timing. the output V1 of the actuation circuit 5 of the 1st switching element 1 -- time of day t4 from -- time amount deltaT2 only -- overdue time of day t5 yes -- since -- it becomes a low. this time of day t5 from -- after the time delay according to the operational characteristic of a switching element,

JP 11-235029 Pg 6 of 20

and time of day t6 a switching element 1 -- off -- becoming -- current I1 and I2 decreasing -- beginning -- current I3 It begins to increase. Time amount deltaT2 Since it has determined that it corresponds to the difference of an actuation time delay in case an actuation time delay and the 3rd switching element 3 in case the 1st switching element 1 is turned off from an ON state are turned on from an OFF state, it is time of day t6. When a switching element 1 becomes off, the switching element 3 is already turned on and current hardly flows through parasitism diode to this switching element 3.

[0013] Generally, the actuation time delay in a switching element is longer than the time of the direction when turning off turning on. Therefore, the timing which the 2nd switching element 2 turns off in this example is time of day t6. Overdue time of day t7 It becomes therefore, current I2 -- time of day t7 up to -- the channel of a switching element 2 can be flowed and it does not flow to parasitism diode Time delay deltaT1 of a delay circuit in case a control signal V4 becomes a high from a low in an above-mentioned example Time delay deltaT2 of a delay circuit in case a control signal V4 becomes a low from a high Although selecting separately, respectively is desirable, even if it makes it the same value, the effect of a considerable degree can be attained. In addition, time delay deltaT2 of a delay circuit in case a control signal V4 becomes a low from a high depending on the configuration of a circuit, an input state, or the property of a switching element It is good also as zero.

[0014] Other examples of this invention are shown in drawing 3. In this example, the control circuit 4 is arranged in the secondary circuit of a transformer 11, and the control signal V4 from this control circuit 4 is directly inputted into the actuation circuits 6 and 7, without passing through an insulating circuit. In respect of others, this example is the same as the example of drawing 1, and the same is said of the actuation. Drawing 4 shows still more nearly another example of this invention. In this example, the current detector 15 is established in the upstream circuit of a transformer 11. It connects with a delay circuit 8, it responds to reduction in the output current, and this current detector 15 is a time delay deltaT1. It becomes large, it responds to the increment in the output current, and is a time delay deltaT1. A delay circuit 8 is controlled to become small. When the load current decreases with the configuration of the example of drawing 1, it is current I3. The time of day and current I1 which become zero from a steadystate value, and I2 The time of day which becomes a steady-state value from zero is t3. It becomes early and is time of day t2. It approaches. However, the time of day which the 3rd switching element 3 turns off is t3. Since it is as, while the switching element 3 is continuing the ON state, switching elements 1 and 2 are turned on. For this reason, in the circuit which passes along the secondary coil of a transformer 11, a short-circuit current flows through switching elements 2 and 3, and it becomes the cause of noise generating in it. Since the example of drawing 4 controls a time delay according to the output current, it can solve this problem. [0015] The trial calculation of the improvement in efficiency which can be attained by the configuration of this invention was made about the specific example. As an assumption, in the conventional circuit, the current between 211 nS(s) flows to the parasitism diode of a switching element, and the voltage drop in parasitism diode is set to 0.9 V by the difference in the delay of a switching element of operation. The specification of a power unit sets V0 =3.3 V, I0 =15A, and drive frequency to 250 kHz, and sets the resistance in the switch-on of a switching element to 5.7mohm. If effectiveness at the time of constituting a rectifier circuit from diode is made into 75%, it is FET about this diode. The effectiveness of synchronous detection mold switching power supply equipment equipped with the rectifier circuit replaced with the switching element of a mold becomes 82.9%, and the effectiveness of the equipment of the example of this

JP 11-235029 Pg 7 of 20

invention shown in <u>drawing 1</u> becomes 83.9%. In this count, only an improvement of the effectiveness acquired by compensating the actuation delay of a switching element among the effects acquired by this invention is taken into consideration. The improvement effect of loss resulting from a short-circuit current is attained, and the noise relief effect is also remarkable in this invention.

[0016] Actuation time delay deltaT2 in the circuit of the specification used for above-mentioned count at drawing 7 It considers as zero and is deltaT1. Change of the effectiveness at the time of making it change and change of a short-circuit current and recovery current are shown. Here, a short-circuit current and recovery current are current I3 which flows the 3rd switching element 3. The current which flows to an arrow head and an opposite direction is pointed out inside. When a time delay is made to increase from this drawing, it turns out that a short-circuit current decreases and effectiveness is improved about 5%. There is also a portion which compensation of the actuation delay of the 2nd switching element 2 contributes in this improvement in efficiency. When a time delay becomes large too much, it is current I3. Since the condition that the 3rd switching element 3 turns off is produced while flowing, it is current I3. Parasitism diode will be flowed and effectiveness falls. It is current I3 to parasitism diode. If the 1st switching element 1 is turned on while flowing, recovery current will flow to the parasitism diode of the 3rd switching element 3. This recovery current increases in proportion to a time delay, and becomes the cause which worsens effectiveness.

[0017] In addition, in the example of <u>drawing 4</u>, although the current detector 15 linked to the primary side circuit of a transformer 11 was used for detection of the load current, this current detector 15 may be established in the secondary circuit of a transformer 11.

JP 11-235029 Pg 8 of 20

# **TECHNICAL FIELD**

[Industrial Application] This invention switches input voltage by the switching means, changes it into high-frequency voltage, and relates to the switching power supply equipment which transforms this high-frequency voltage with a transformer, rectifies and outputs the output voltage of arbitration. Especially this invention establishes a switching means as a rectifying device of the rectifier circuit of the output section, and relates to the synchronous detection mold switching power supply equipment it was made to operate this switching means synchronizing with actuation of the switching means of an input circuit.

JP 11-235029 Pg 9 of 20

### PRIOR ART

[Description of the Prior Art] Input voltage is changed into high-frequency voltage by the switching means, it is impressed by the primary coil of a transformer, and the switching power supply equipment which took out the secondary coil of this transformer from the output circuit which has a rectifier circuit as a dc output is known well. In this switching power supply equipment, it connects with a rectifying device, magnetic cells, such as a coil, and secondary coils, such as diode connected to the secondary coil of a transformer at the serial, at juxtaposition, and a rectifier circuit is equipped with another rectifying device. On-off control of the switching means of an input side is carried out by the control signal from a control circuit so that output voltage may serve as a predetermined value. In the switching power supply equipment of this format, in order to mitigate loss by the forward drop voltage of a proper to diode, it replaces with diode and a switching device is used, the configuration which these switching devices are synchronized with the switching means of an input side, and was made to carry out on-off control is known as a synchronous detection mold switch power unit, and the typical thing of the switch power unit of such format is indicated by JP,4-4750,A, JP,5-260738,A and JP,7-194104,A, and the list at the U.S. Pat. No. 4,870,555 description.

[0003] An example of the conventional synchronous detection mold switch power unit is shown in drawing 5. In drawing 5, a power supply 13 is connected to primary-winding 11a of a transformer 11, and the switching device 1 of an FET mold is further connected to this primarywinding 11a. The output circuit 14 which has a rectifier circuit 12 is connected to secondary coil 11b of a transformer 11, and this output circuit 14 is connected to a load 15. A rectifier circuit 12 is equipped with 2nd switching device 2 and magnetic cell, i.e., inductor, 12a connected to secondary-winding 11b of a transformer 11 at the serial. Moreover, a rectifier circuit 12 is equipped with the 3rd switching device 3 connected to juxtaposition at secondary-winding 11b of a transformer 11. In order to control switching devices 1, 2, and 3, the control circuit 4 is formed. It connects with the output circuit 14 through the insulating circuit 9 or the load voltage detector 10 which consists of a photo coupler or a transformer, and a control circuit 4 outputs the control signal V4 for controlling a switching device 1 which modulated pulse width so that output voltage might become fixed. The output V4 of a control circuit 4 is impressed to the gate electrode of the 1st switching device 1 as an output V1 through the actuation circuit 5. The control signal V4 from a control circuit 4 is connected to the actuation circuits 6 and 7 again through the insulating circuit 9 which consisted of a transformer or a photo coupler. The actuation circuit 6 impresses the same polar output V2 as the output V1 impressed to the 1st switching device 1 to the gate electrode of the 2nd switching device 2. The actuation circuit 7 impresses the output V3 of reversed polarity to the gate electrode of the 3rd switching device 3 with the output V1 impressed to the 1st switching device 1.

[0004] As everyone knows, on-off control of the 1st switching device 1 is carried out by the control signal from a control circuit 4, voltage from a power supply 13 is made into high-frequency voltage, and this high-frequency voltage is impressed to the primary winding of a transformer 11. It is rectified by the rectifier circuit 12 and the voltage generated in secondary-winding 11b of a transformer 11 is outputted from an output circuit 14. The output voltage of an output circuit 14 is detected by the load voltage detector 10, and is inputted into a control circuit 4. A control circuit 4 generates the control signal for controlling the 1st switching device 1 so that output voltage serves as a predetermined value. In a rectifier circuit 12, when the 1st

JP 11-235029 Pg 10 of 20

switching device 1 is an ON state, the 2nd switching device 2 will also be in an ON state, and the 3rd switching device 3 is turned off. If the 1st switching device 1 becomes off, the 2 switching devices 2 of \*\* will also become off, and the 3rd switching device 3 will be turned on. [0005] Here, when a control signal is impressed to the same timing as the 1st, 2nd, and 3rd switching device 1, 2, and 3, a gap is produced to timing of operation between each switching device for the operational characteristic of FET which constitutes a switching device. That is, there is a time delay of operation after the voltage impressed to a time delay of operation and a gate electrode until the drain current which flows this switching device after driver voltage is impressed to the gate electrode of a switching device reaches a steady-state value is severed until drain current will not flow. The effectiveness of switching power supply equipment falls for this time delay. If this point is explained to details, since voltage of an input side is high, generally FET which constitutes the switching device 1 of an input side will have comparatively high pressure-proofing, and what has small current capacity will be used. Therefore, this switching device 1 has a comparatively short time delay after a time delay and driver voltage after driver voltage is impressed to a gate electrode until it will be in an ON state are removed until it will be in an OFF state. On the other hand, voltage of an output side is low and, generally, as for FET which constitutes the switching devices 2 and 3 of an output side, the thing with low pressureproofing which has large current capacity is used. For this reason, in these switching devices 2 and 3, a time delay after a time delay and driver voltage after driver voltage is impressed to a gate electrode until it will be in an ON state are removed until it will be in an OFF state is comparatively long.

[0006] The voltage or the current wave form of each part of switching power supply equipment shown in drawing 5 is shown in drawing 6. Time of day to If a control signal V4 becomes a high from a low, the output V1 from the actuation circuit 5 and the output V2 from the actuation circuit 6 will become a high simultaneously. Moreover, the output V3 from the actuation circuit 7 becomes a low to the same timing, this time of day to from -- after the time delay according to the operational characteristic of a switching element, and time of day t1 A switching element 1 is turned on and current I1 flows to upstream coil 11a of a transformer 11. Simultaneously, it is current I2 to secondary coil 11b of a transformer 11. It generates. Current I3 which was flowing to the switching element 3 by the OFF state of a switching element 1 Time of day t1 It begins to decrease and is time of day t2. It becomes zero. On the property of an element, since the actuation time delay of a switching element 3 is longer than the time delay of a switching element 1, at this event, a switching element 3 is still in an ON state. Therefore, secondarywinding 11b of a transformer 11 will be in a short circuit condition through switching elements 2 and 3, and a big short-circuit current flows and it causes degradation and a noise. Moreover, since the actuation time delay is longer than a switching element 1, at this event, a switching element 2 also has a switching element 2 in an OFF state. Therefore, since the short-circuit current which flows through this switching element 2 will pass not along the channel between the drain sources but along internal parasitism diode, loss becomes large. It sets to drawing 6 and is current I2. A slash shows the current which flows to parasitism diode inside. [0007] Time of day t3 If a control signal V4 becomes a low from a high, the output V1 from the actuation circuit 5 and the output V2 from the actuation circuit 6 will become a low. The output V3 of an actuation circuit becomes a high from a low to the same timing, time of day t3 from -after the time delay according to the operational characteristic of a switching element, and time of day t4 a switching element 1 -- off -- becoming -- current I1 and I2 decreasing -- beginning -current I3 It begins to increase. Since a switching element 3 still is not an ON state at this time,

JP 11-235029 Pg 11 of 20

to this switching element 3, current comes to flow through parasitism diode, and loss becomes large. To <u>drawing 6</u>, it is current I3. A look shows the current which flows to parasitism diode inside.

JP 11-235029 Pg 12 of 20

# TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] This invention makes it to offer the switching power supply equipment which can control the loss by difference of the actuation time delay of the switching element of a switching circuit and the switching element of a rectifier circuit, and generating of a noise the technical problem which should be solved in the synchronous detection mold switching telegraph-key equipment of the format mentioned above.

JP 11-235029 Pg 13 of 20

### **MEANS**

[Means for Solving the Problem] Switching power supply equipment by this invention for solving the above-mentioned technical problem A switching circuit which has the 1st switching means which changes input voltage into high-frequency voltage, It has \*\*\*\*\*\* by which a primary coil was connected to this switching circuit, and a secondary coil was connected to an output circuit. This output circuit The 2nd switching means and magnetic cell which were connected to a secondary coil of a transformer at a serial, It has a rectification means which becomes a secondary coil from the 3rd switching means connected to juxtaposition. A control means which forms a control signal given to this 1st switching means in order to carry out on-off control of the 1st switching means so that output voltage may serve as a predetermined value is established. On-off control of the 2nd switching means is carried out by signal from a control means which synchronized with a control signal given to the 1st switching means. A control signal with which the 3rd switching means is given to the 1st switching means is equipment of a synchronous detection mold by which on-off control came to be carried out by signal from a control means which has timing of reverse. A power unit of this invention has a signal timing adjustment means to make it timing as which a control signal is inputted into the 1st switching means rather than timing as which a control signal is inputted into the 2nd and 3rd switching means become late in order to compensate a difference of an actuation time delay based on a resisting pressure property between the 1st switching means and the 2nd and 3rd switching means, or a difference of current capacity as the feature. As for this signal timing adjustment means, it is most desirable to constitute as a delay means to delay timing of a control signal inputted into the 1st switching means. In this case, as for this delay means, it is desirable to enable it to set up independently a time delay over an ON signal to the 1st switching means and a time delay over an off signal. A load current detection means is established and it is made for a time delay over an ON signal to the 1st switching means to be changed in a still more desirable mode of this invention according to magnitude of the load current.

[0010] In switching power supply equipment of this invention as mentioned above with a signal timing adjustment means In order to compensate a difference of an actuation time delay based on a difference of a resisting pressure property between the 1st switching means and the 2nd and 3rd switching means Since it adjusts so that timing as which a control signal is inputted into the 1st switching means rather than timing as which a control signal is inputted into the 2nd and 3rd switching means may become late On--off timing of the 1st, 2nd, and 3rd switching element can be synchronized thoroughly, current which flows to parasitism diode of a switching element can be decreased, loss can be reduced, and generating of a noise can be controlled.

JP 11-235029 Pg 14 of 20

### **EXAMPLE**

[Example] Hereafter, the example of this invention is explained about drawing. If <u>drawing 1</u> is referred to first, the circuit of the example shown here is almost the same as that also of the conventional circuit shown in drawing 5, and a configuration and an operation, and a corresponding portion will attach the same agreement and will omit detailed explanation. In the circuit of this example, a delay circuit 8 is arranged in the circuit from the control circuit 4 to the actuation circuit 5 of the 1st switching element 1. The insulating circuit 9 connected to the actuation circuits 6 and 7 of the 2nd and 3rd switching element 2 and 3 is connected to a control circuit 4 between a control circuit 4 and a delay circuit 8. Therefore, although the direct input of the control signal V4 from a control circuit 4 is carried out to the actuation circuits 6 and 7, it is inputted into the actuation circuit 5 through a delay circuit 8. The voltage or the current wave form of each part of a circuit shown in drawing 2 at drawing 1 is shown. Time of day to If a control signal V4 becomes a high from a low, the output V2 from the actuation circuit 6 will become a high, and the output V3 from the actuation circuit 7 will become a low to the same timing simultaneously, the actuation circuit 5 of the 1st switching element 1 -- a control signal V4 -- time amount deltaT1 only -- since it is behind and is inputted -- output V1 of the actuation circuit 5 Time of day to Time amount deltaT1 only -- overdue time of day t1 from a low -- yes, it comes to be alike a switching element 1 -- time of day to from -- after the time delay according to the operating characteristic of this switching element, and time of day t2 ON -- becoming -current I1 Primary-winding 11a of a transformer 11 flowing -- simultaneous -- secondarywinding 11b of a transformer 11 Current I2 It generates. Current I3 which was flowing to the switching element 3 by the OFF state of a switching element 1 Time of day t2 It begins to decrease and is time of day t3. It becomes zero. Time of day t3 It is current I1 and I2 then. A steady-state value is reached. a switching element 3 -- time of day to from -- after the time delay according to the operational characteristic of this switching element, and time of day t3 It turns off. \*\*T1 Time of day t3 It is determined that a switching device 3 turns off. Since the time amount which the direction when turning off the actuation time delay in a switching element turns on is generally long, a switching element 2 is time of day t2. It is turned on when early. [0012] It sets in this circuit and is time of day t3. Current I3 Since the 3rd switching element 3 also becomes off when becoming zero, it can prevent that a short-circuit current flows to secondary-winding 11b of a transformer 11. current I2 Time of day t2 which begins to flow by -since the 2nd switching element 2 is turned on -- current I2 Flowing the channel between the drain sources of an element 2, to parasitism diode, current hardly flows. Thus, in this example of this invention, loss can be reduced and a noise can be decreased. Time of day t4 If a control signal V4 becomes a low from a high, the output V2 of the actuation circuit 6 will become a low. The output V3 of an actuation circuit also becomes a high from a low to the same timing, the output V1 of the actuation circuit 5 of the 1st switching element 1 -- time of day t4 from -- time amount deltaT2 only -- overdue time of day t5 yes -- since -- it becomes a low. this time of day t5 from -- after the time delay according to the operational characteristic of a switching element, and time of day to a switching element 1 -- off -- becoming -- current I1 and I2 decreasing -beginning -- current I3 It begins to increase. Time amount deltaT2 Since it has determined that it corresponds to the difference of an actuation time delay in case an actuation time delay and the 3rd switching element 3 in case the 1st switching element 1 is turned off from an ON state are turned on from an OFF state, it is time of day to. When a switching element 1 becomes off, the

JP 11-235029 Pg 15 of 20

switching element 3 is already turned on and current hardly flows through parasitism diode to this switching element 3.

[0013] Generally, the actuation time delay in a switching element is longer than the time of the direction when turning off turning on. Therefore, the timing which the 2nd switching element 2 turns off in this example is time of day t6. Overdue time of day t7 It becomes therefore, current I2 -- time of day t7 up to -- the channel of a switching element 2 can be flowed and it does not flow to parasitism diode Time delay deltaT1 of a delay circuit in case a control signal V4 becomes a high from a low in an above-mentioned example Time delay deltaT2 of a delay circuit in case a control signal V4 becomes a low from a high Although selecting separately, respectively is desirable, even if it makes it the same value, the effect of a considerable degree can be attained. In addition, time delay deltaT2 of a delay circuit in case a control signal V4 becomes a low from a high depending on the configuration of a circuit, an input state, or the property of a switching element It is good also as zero.

[0014] Other examples of this invention are shown in drawing 3. In this example, the control circuit 4 is arranged in the secondary circuit of a transformer 11, and the control signal V4 from this control circuit 4 is directly inputted into the actuation circuits 6 and 7, without passing through an insulating circuit. In respect of others, this example is the same as the example of drawing 1, and the same is said of the actuation. Drawing 4 shows still more nearly another example of this invention. In this example, the current detector 15 is established in the upstream circuit of a transformer 11. It connects with a delay circuit 8, it responds to reduction in the output current, and this current detector 15 is a time delay deltaT1. It becomes large, it responds to the increment in the output current, and is a time delay deltaT1. A delay circuit 8 is controlled to become small. When the load current decreases with the configuration of the example of drawing 1, it is current I3. The time of day and current I1 which become zero from a steadystate value, and I2 The time of day which becomes a steady-state value from zero is t3. It becomes early and is time of day t2. It approaches. However, the time of day which the 3rd switching element 3 turns off is t3. Since it is as, while the switching element 3 is continuing the ON state, switching elements 1 and 2 are turned on. For this reason, in the circuit which passes along the secondary coil of a transformer 11, a short-circuit current flows through switching elements 2 and 3, and it becomes the cause of noise generating in it. Since the example of drawing 4 controls a time delay according to the output current, it can solve this problem. [0015] The trial calculation of the improvement in efficiency which can be attained by the configuration of this invention was made about the specific example. As an assumption, in the conventional circuit, the current between 211 nS(s) flows to the parasitism diode of a switching element, and the voltage drop in parasitism diode is set to 0.9 V by the difference in the delay of a switching element of operation. The specification of a power unit sets V0 =3.3 V, I0 =15A, and drive frequency to 250 kHz, and sets the resistance in the switch-on of a switching element to 5.7mohm. If effectiveness at the time of constituting a rectifier circuit from diode is made into 75%, it is FET about this diode. The effectiveness of synchronous detection mold switching power supply equipment equipped with the rectifier circuit replaced with the switching element of a mold becomes 82.9%, and the effectiveness of the equipment of the example of this invention shown in drawing 1 becomes 83.9%. In this count, only an improvement of the effectiveness acquired by compensating the actuation delay of a switching element among the effects acquired by this invention is taken into consideration. The improvement effect of loss resulting from a short-circuit current is attained, and the noise relief effect is also remarkable in this invention.

JP 11-235029 Pg 16 of 20

[0016] Actuation time delay deltaT2 in the circuit of the specification used for above-mentioned count at drawing 7 It considers as zero and is deltaT1. Change of the effectiveness at the time of making it change and change of a short-circuit current and recovery current are shown. Here, a short-circuit current and recovery current are current I3 which flows the 3rd switching element 3. The current which flows to an arrow head and an opposite direction is pointed out inside. When a time delay is made to increase from this drawing, it turns out that a short-circuit current decreases and effectiveness is improved about 5%. There is also a portion which compensation of the actuation delay of the 2nd switching element 2 contributes in this improvement in efficiency. When a time delay becomes large too much, it is current I3. Since the condition that the 3rd switching element 3 turns off is produced while flowing, it is current I3. Parasitism diode will be flowed and effectiveness falls. It is current I3 to parasitism diode. If the 1st switching element 1 is turned on while flowing, recovery current will flow to the parasitism diode of the 3rd switching element 3. This recovery current increases in proportion to a time delay, and becomes the cause which worsens effectiveness.

[0017] In addition, in the example of <u>drawing 4</u>, although the current detector 15 linked to the primary side circuit of a transformer 11 was used for detection of the load current, this current detector 15 may be established in the secondary circuit of a transformer 11.

JP 11-235029 Pg 17 of 20

### DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the circuit diagram showing the switching power supply equipment by one example of this invention.

[Drawing 2] It is the wave form chart showing the voltage of each part in the circuit of <u>drawing</u> 1, or the wave of current.

[Drawing 3] It is the same circuit diagram as <u>drawing 1</u> which shows the switching power supply equipment by other examples of this invention.

[Drawing 4] It is the same circuit diagram as <u>drawing 1</u> which shows the switching power supply equipment by the example of further others of this invention.

[Drawing 5] It is the same circuit diagram as <u>drawing 1</u> which shows an example of conventional synchronous detection mold switching power supply equipment.

[Drawing 6] It is drawing showing the wave of each part in the circuit of drawing 5.

[Drawing 7] It is the chart showing change of an improvement of the effectiveness acquired by this invention by the time delay in an example, a short-circuit current, and recovery current. [Explanation of agreement]

1, 2, 3 [ ... A delay circuit, 9 / ... An insulating circuit 10 / ... A load voltage detector, 11 / ... A transformer, 12 / ... A rectifier circuit, 13 / ... A power supply, 14 / ... An output circuit, 15 / ... Load ] ... A switching element, 4 ... A control circuit, 5, 6, 7 ... An actuation circuit, 8

JP 11-235029 Pg 18 of 20

### CORRECTION OR AMENDMENT

[Official Gazette Type] Printing of amendment by the convention of 2 of Article 17 of patent law [Category partition] The 4th partition of the 7th category [Date of issue] June 22, Heisei 13 (2001. 6.22)

[Publication No.] JP,11-235029,A

[Date of Publication] August 27, Heisei 11 (1999. 8.27)

[Year copy format] Open patent official report 11-2351

[Filing Number] Japanese Patent Application No. 10-35740

[The 7th edition of International Patent Classification]

H02M 3/28

3/335

7/21

[FI]

H02M 3/28 F

3/335 B

7/21 A

[Procedure amendment]

[Filing Date] November 16, Heisei 11 (1999. 11.16)

[Procedure amendment 1]

[Document to be Amended] Description

[Item(s) to be Amended] Claim

[Method of Amendment] Modification

[Proposed Amendment]

[Claim(s)]

[Claim 1] A switching circuit which has the 1st switching means which changes input voltage into high-frequency voltage,

\*\*\*\*\*\* by which a primary coil was connected to said switching circuit, and a secondary coil was connected to an output circuit,

A preparation and said output circuit have a rectification means which becomes the 2nd switching means and a magnetic cell which were connected to said secondary coil of said transformer at a serial, and said secondary coil from the 3rd switching means connected to juxtaposition,

In order to carry out on-off control of said 1st switching means so that output voltage may serve as a predetermined value, a control means which forms a control signal given to said 1st switching means is established,

On-off control of said 2nd switching means is carried out by signal from said control means which synchronized with a control signal given to said 1st switching means,

A control signal with which said 3rd switching means is given to said 1st switching means is a synchronous detection mold power unit by which on-off control came to be carried out by signal

JP 11-235029 Pg 19 of 20

from said control means which has timing of reverse,

Synchronous detection mold switching power supply equipment characterized by what a signal timing adjustment means to make it timing as which a control signal is inputted into said 1st switching means rather than timing as which a control signal is inputted into said 2nd and 3rd switching means in order to compensate a difference of an actuation time delay based on said 1st switching means, said 2nd [ the ] and a resisting pressure property between said 3rd switching means, or a difference of current capacity become late was established for.

[Claim 2] It is switching power supply equipment characterized by being a delay means to delay the timing of a control signal of being switching power supply equipment indicated to claim 1, and inputting said signal timing adjustment means into said 1st switching means.

[Claim 3] It is switching power supply equipment characterized by the ability to set up now independently a time delay [ as opposed to / are switching power supply equipment indicated to claim 2, and / an ON signal to said 1st switching means in said delay means ], and a time delay over an off signal.

[Claim 4] Switching power supply equipment characterized by being switching power supply equipment indicated to claim 3, establishing a load current detection means, and coming to change a time delay over an ON signal to said 1st switching means according to magnitude of the load current.

JP 11-235029 Pg 20 of 20